Ultra-Low Power UWB Concepts

Advanced Signal Processing Seminar SS09

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- UWB Wireless Sensor Networks
- 1st design: UWB WSN
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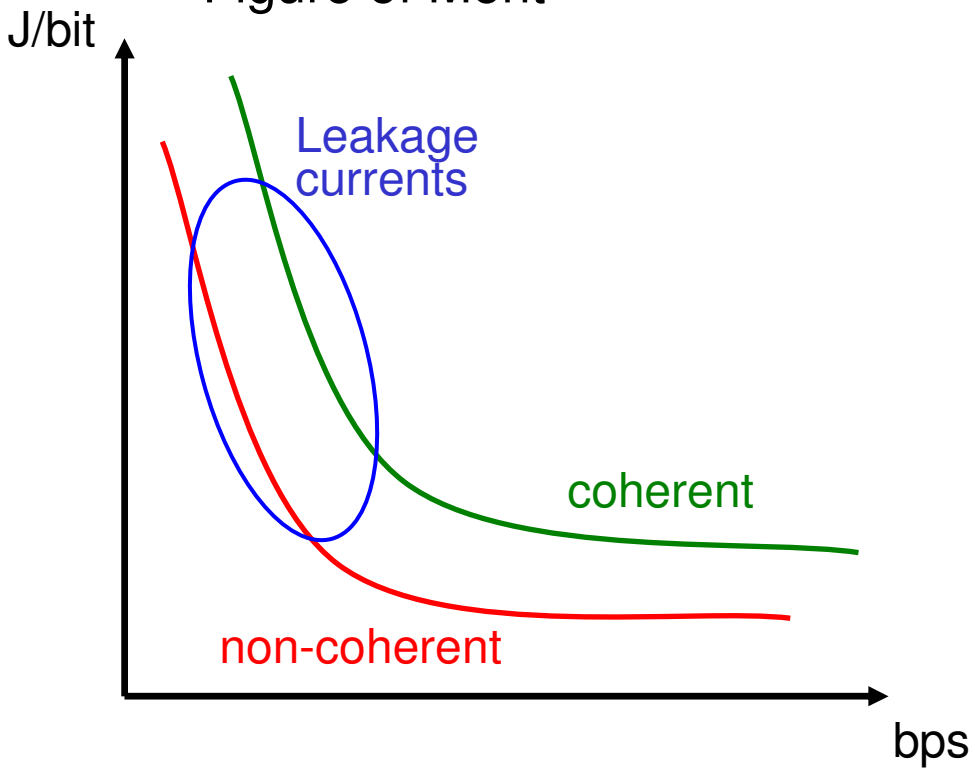
Introduction and Motivation

- Wireless Sensor Networks (WSNs), Body Area Networks (BANs) and Ultra-Low-Power RFID tags require Low-Power consumption
- UWB receivers consume more energy than transmitters therefore we'll focus on receivers
- There is (yet) a huge complexity needed to build a *coherent* UWB receiver
  - ADC's and DSP's have to operate on a huge bandwidth and are power hungry
- Tradeoff between *coherent* and *non-coherent* receiver design
  - Efficient bandwidth usage and better sensitivity vs. low data rate and energy efficiency

Introduction and Motivation

- CMOS process technology has influence on the power consumption
- Figure of Merit



Data-rate independent Energy per Bit area

Low Energy/Bit ratio

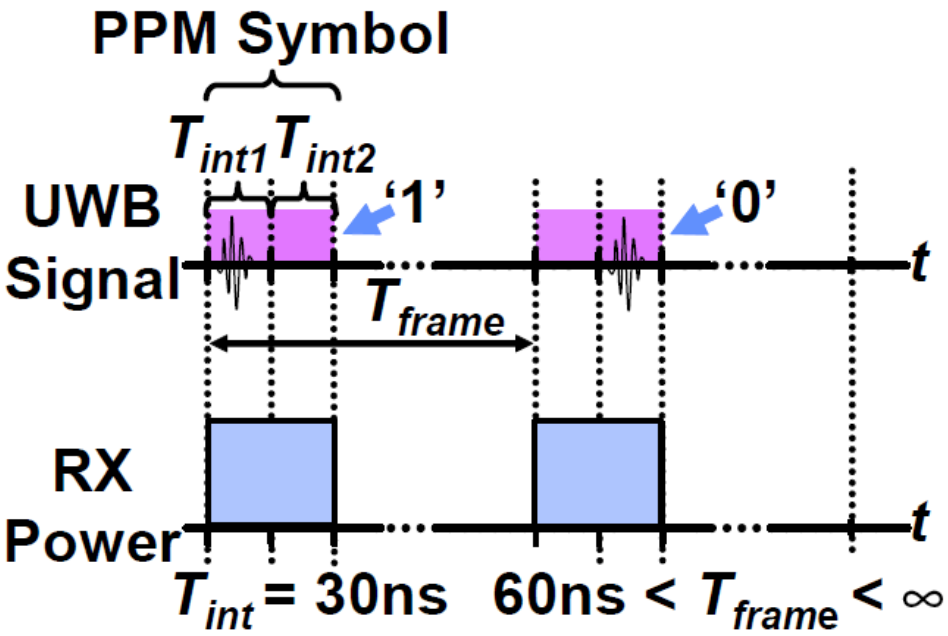
Sub nJ/bit at ≥10 kbps

Non coherent receiver characteristics

- Recover only the signal envelope not the phase information
- Energy detector architecture
- Suboptimal spectral efficiency
- OOK, PPM used, PSK types useless because of the loss of the phase
- No PLL, correlators and template-signal generators needed
- Pulse Position Modulation Schemes

Pulse Position Modulation

- The position of the pulse contains the information
- No phase required
- Used in optical systems
- PPM data-rate is restricted by delay-spread



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UWB Wireless Sensor Networks

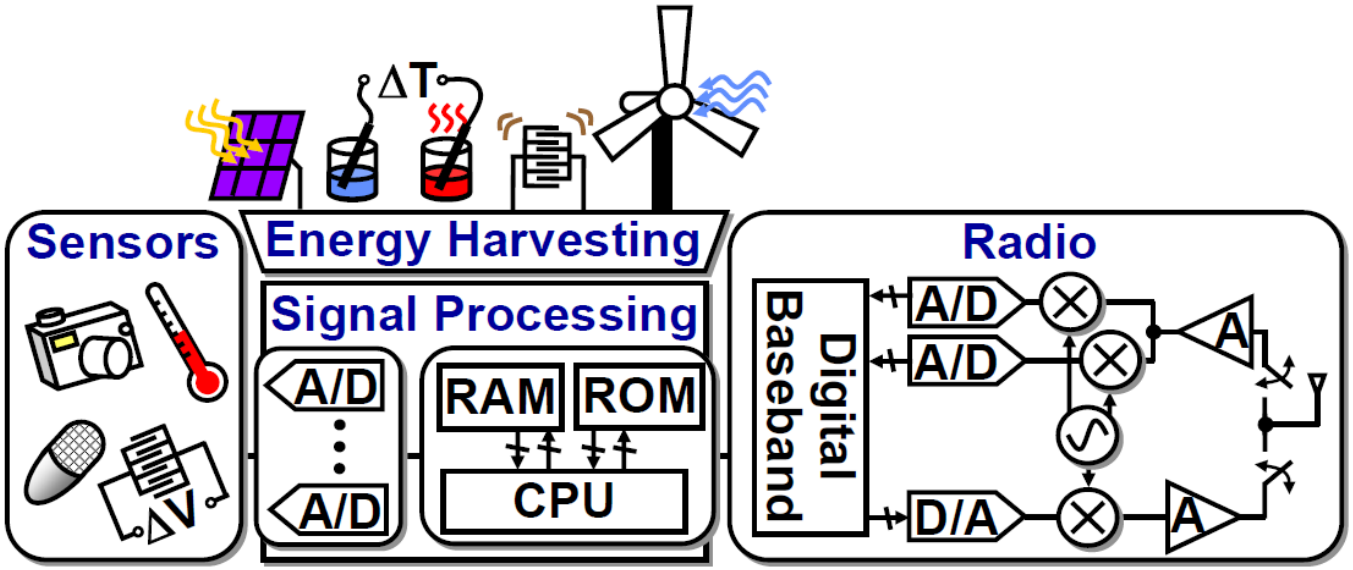
- Typical Specifications

Data Rate	kbps to Mbps
Spatial Density	0.1 – 10 nodes/m²
Transmit distance	10 – 100 m
Extended Lifetime	>= 5 Years
Small size	1 „AA“ Battery

“The average power consumption must be less than 85 µW”

- Typical Architecture is a Transceiver architecture with transmitter and receiver in one tag/node
- Future: Transceiver in one SoC

Wireless Sensor Network Transceivers



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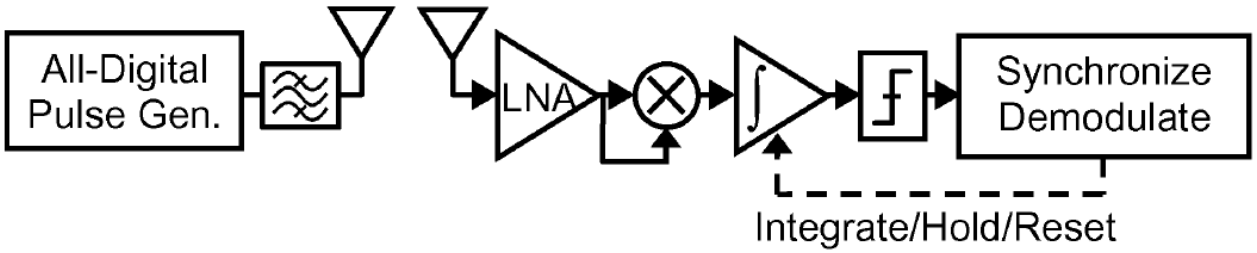
Simple architecture

Low data rate

Low power consumption

Typical low power transceiver design



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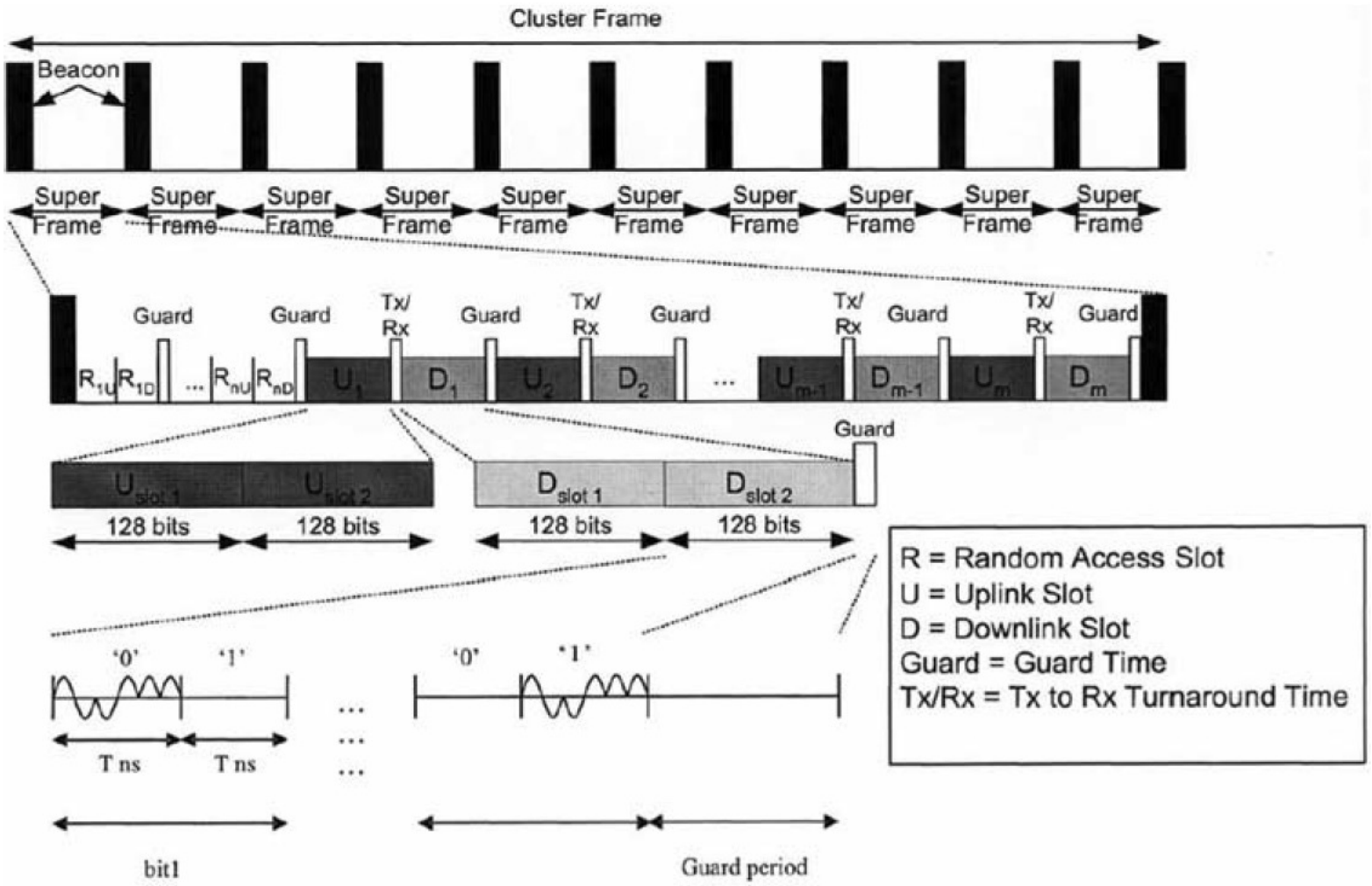
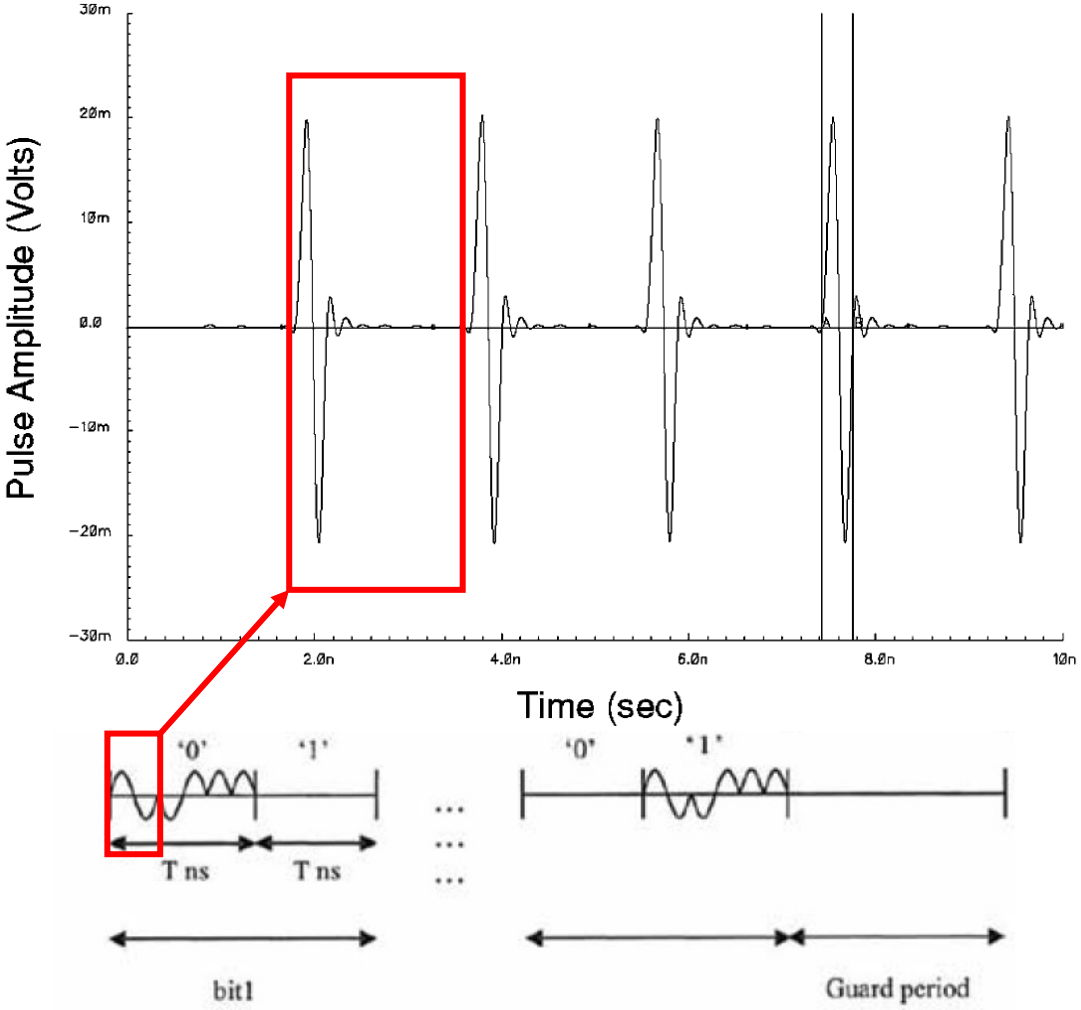
1st proposed WSN design

- By University of Oulu in 2005
- Tag based architecture
- UWB-IR with BPPM 5 MBit/s
- Additional Direct sequence spreading
- 340 ps wide pulses
- 1 GHz Bandwidth
- Low duty cycle signaling
- Max. Tag distance: 50m, max. Tag speed: 60 km/h
- 0.35µm CMOS (BiCMOS) process technology
- Separation of Users in time domain (TDMA/TDD)
- up to 1000 Tags
- Master/Slave Configuration (Central Station, Fixed Nodes, Tags)

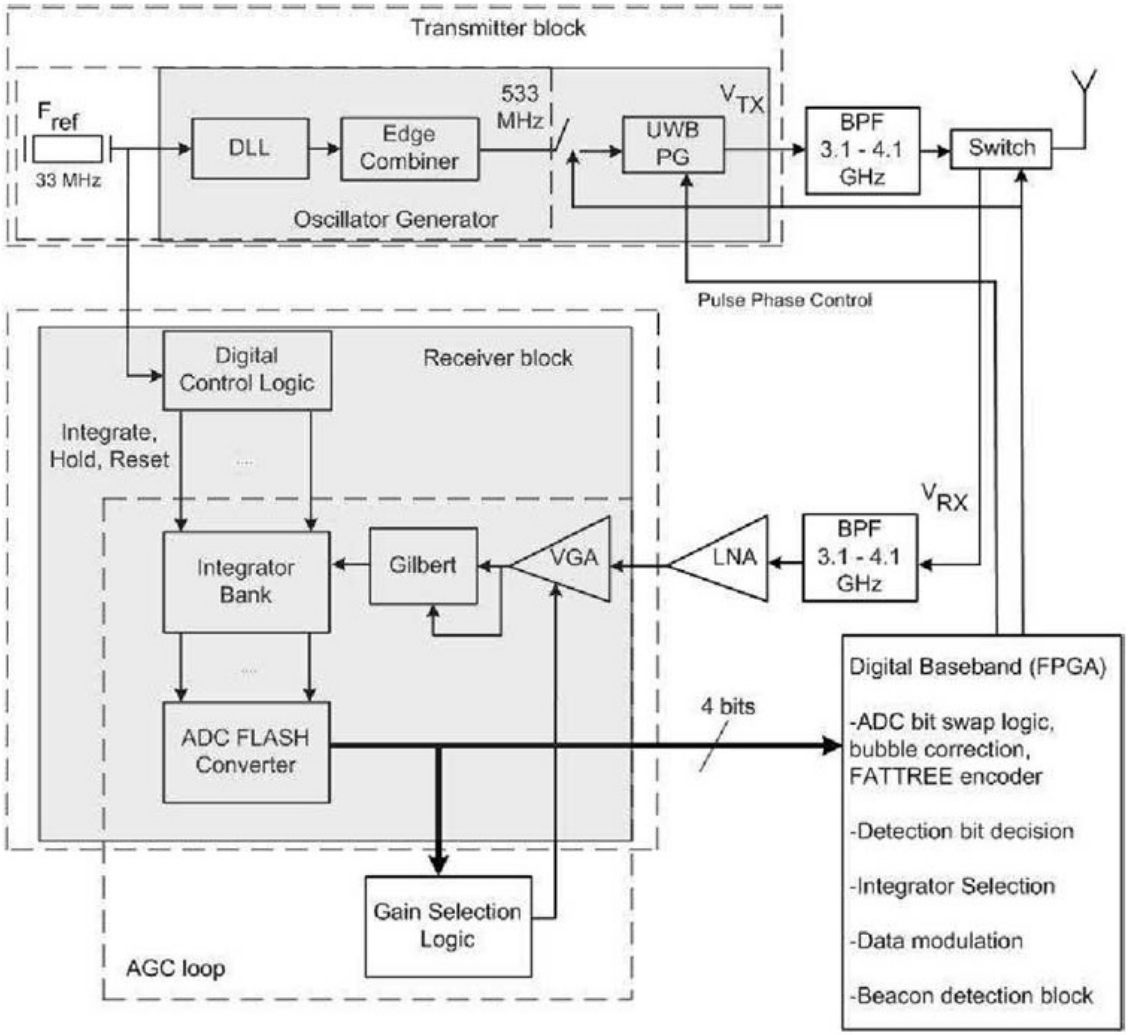
MAC Layer


Cluster Frame
Beacon
Super Frame
Guard
Tx/Rx
128 bits
'0'
'1'
T ns
bit1
Guard period
R = Random Access Slot
U = Uplink Slot
D = Downlink Slot
Guard = Guard Time
Tx/Rx = Tx to Rx Turnaround Time

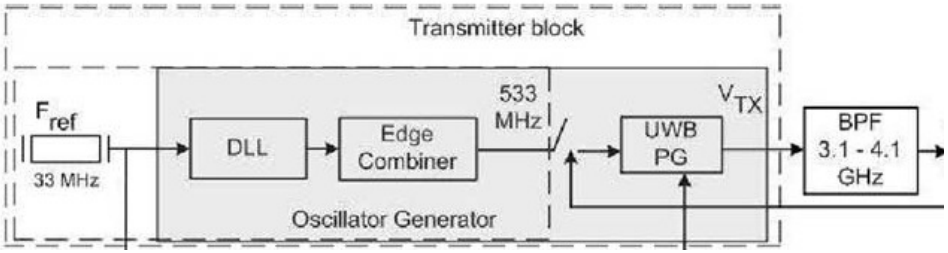
MAC Layer


Pulse Amplitude (Volts)
30m
20m
10m
0.0
−10m
−20m
−30m
0.0
2.0n
4.0n
6.0n
8.0n
10n
Time (sec)
'0'
'1'
T ns
T ns
bit1
'0'
'1'
Guard period

1st proposed WSN design (Transceiver)



1st proposed WSN design (Transmitter)



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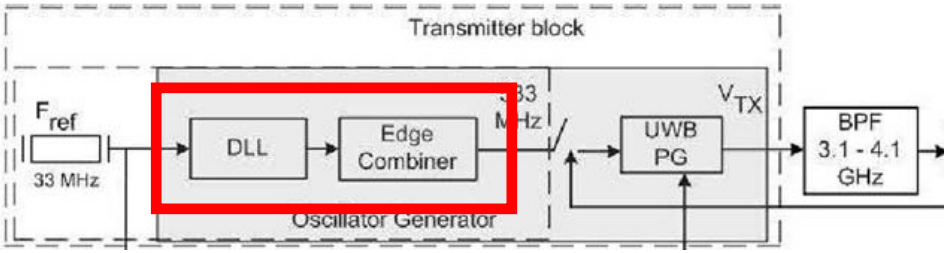

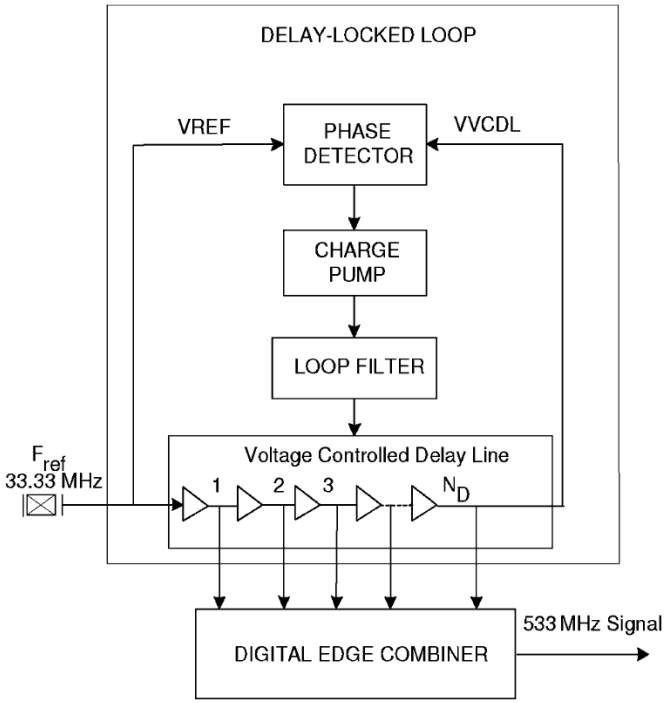

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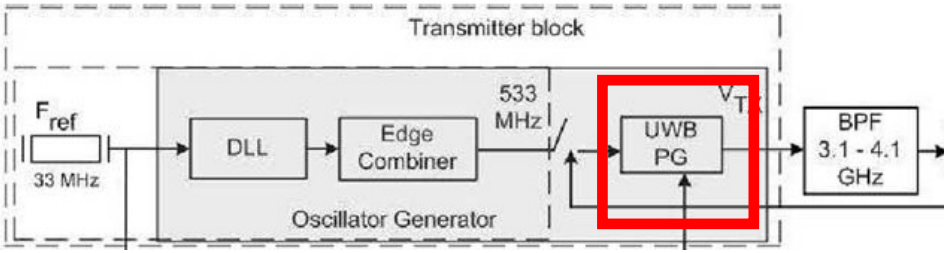
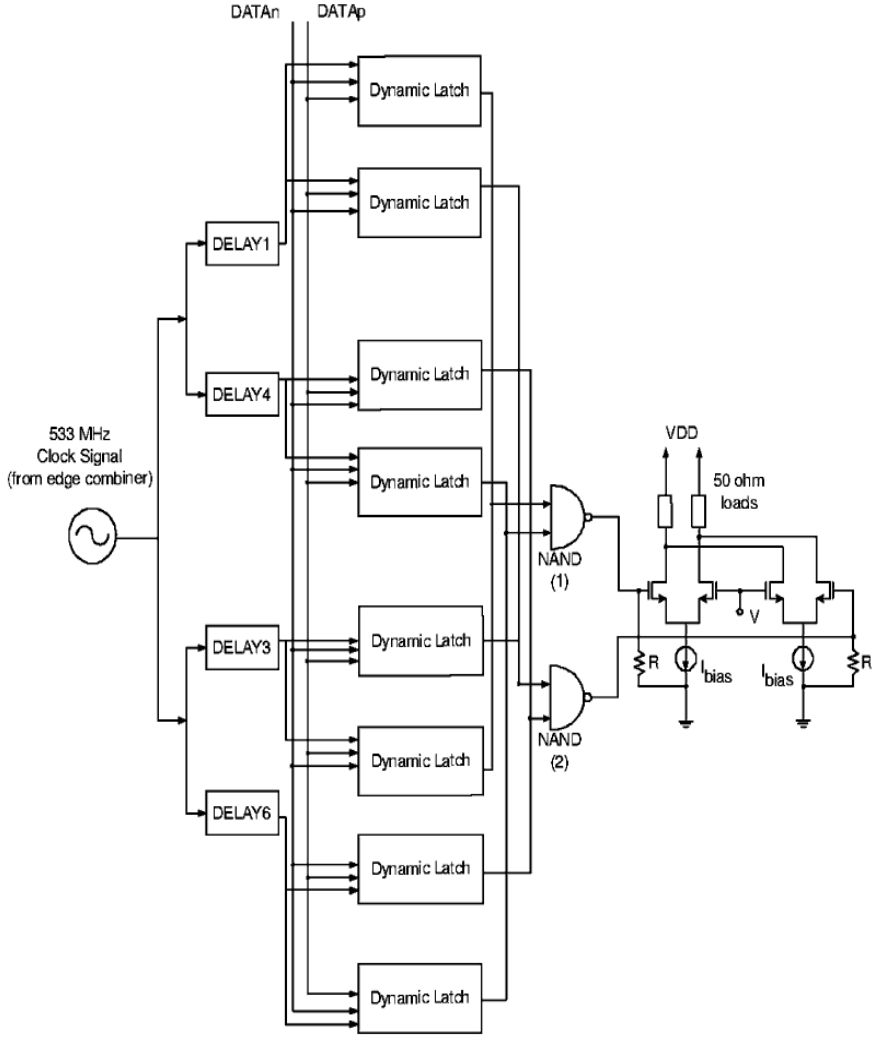
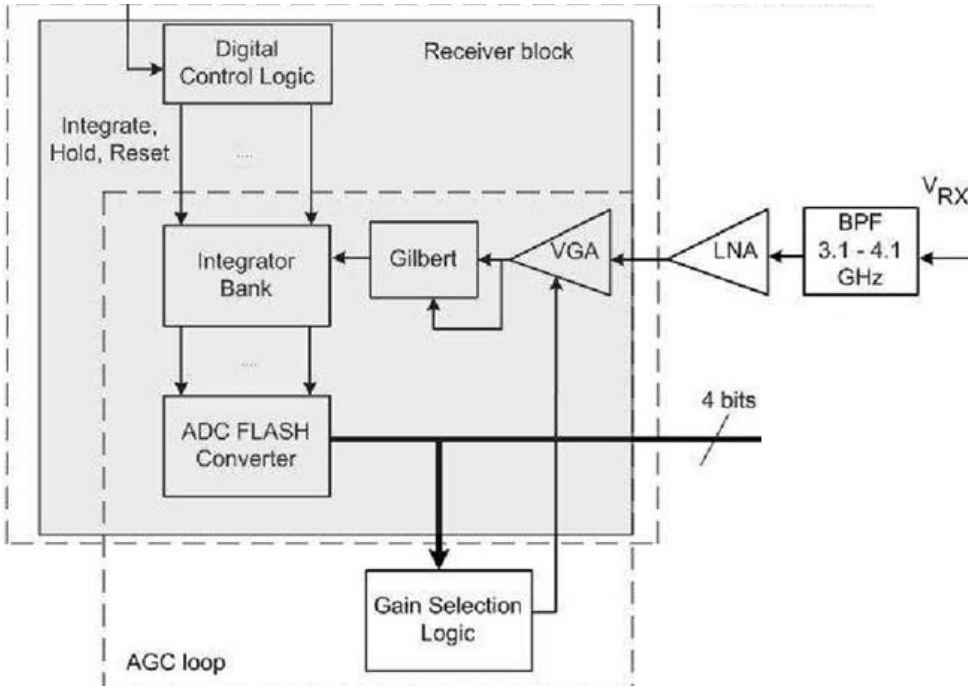




1st proposed WSN design (Receiver)



BPF: 1 GHz

LNA: 7,5 dB

VGA: -5 to 15 dB

Gilbert multiplier

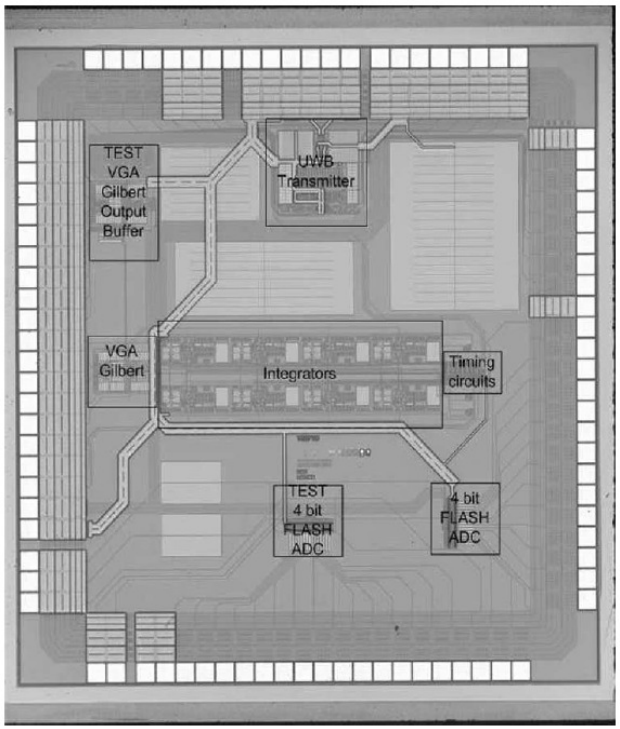
Integrators based on Operational transconductance amplifiers (OTA)

4Bit Flash ADC: 33 MSa/s

Energy consumption analysis

- VGA: 3.2 mA
- Pulse generator: 8.3 mA
- 8 Integrators: 24 mA
- Total current consumption: 39.6 mA
- At 3.3 V results in 136 mW at 100% duty cycle

- The 8 integrators allow very precise synchronization, but consume 68% of the energy
- If localization is not an issue there is a lot of space for power reduction

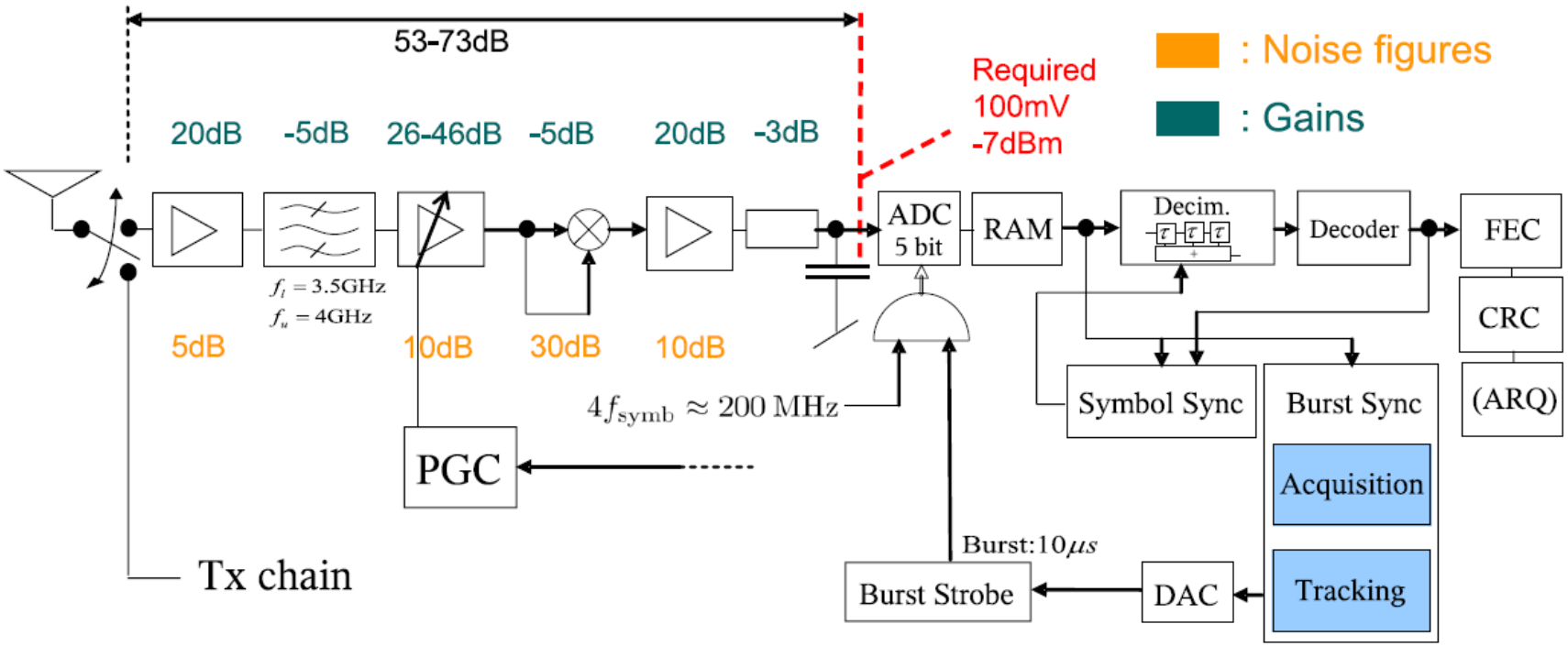


[Stoi]

Improvement of the receiver architecture

- New goal: Body Area Network without positioning
  → relaxed requirements regarding synchronization
- By ETH Zürich in 2007
- 500 MHz Bandwidth (3.5 GHz – 4 GHz)
- Bursts of 10µs every 1ms
- FCC compliant average power: -14.26 dBm
- Delay spread of 10 to 50 ns (Indoor scenarios)
  → max data rate: 50 Mbps

New receiver architecture



[Troe]

- 1st order LPF instead of integrators
- LNA before BPF

Low duty cycle signaling

- An SNR of 10.5 dB is required over an AWGN channel to acheive a BER of 10^{-3}
- We consider a path loss (PL) of 60 dB, an Implementation loss (F) of 10 dB and a thermal noise floor N_0 of -174 dB/Hz
- This corresponds to a transmit energy/bit

$$E_{\mathrm{b,tx}} = N_0 + PL + F + \mathrm{SNR}_{\mathrm{ref}} = -93.5 \text{ dBm/Hz}$$

- The minimal transmit power to acheive a BER of 10^{-3} for f_b = 500 kbps is

$$P_{\mathrm{tx}} = E_{\mathrm{b,tx}} + 10\log_{10}(f_{\mathrm{B}}) = -36.5 \text{ dBm}$$

- But FCC allows only -101 dBm/Hz therefore our min. BW is

$$10\log_{10}(B_{\min}) = P_{\mathrm{tx}} - E_{\mathrm{av,max}} = 64.5 \text{ dBHz} \mathrel{\widehat{=}} 2.8 \text{ MHz}$$

Low duty cycle signaling

- Increasing the BW allows to transmit at a higher rate

$$f_{\mathrm{B,max}} = \frac{B}{B_{\mathrm{min}}} f_{\mathrm{B}} = \frac{1}{\eta} f_{\mathrm{B}}$$

- With a BW of 500 MHz we would acheive ~90Mbps, but to avoid ISI we have to take care of the delay-spread
- For indoor channels we get

$$f_{\mathrm{B,max}} \approx \frac{1}{2\tau_{\mathrm{rms}}} \in [10; 50] \ \ \mathrm{Mbps}$$

- And a min. duty-cycle of

$$\eta_{\mathrm{min}} = \frac{f_{\mathrm{B}}}{f_{\mathrm{B,max}}} = \frac{500 \text{ kbps}}{50 \text{ Mbps}} = 0.01 = 1\%$$

Energy Consumption for duty cycling

- T_{burst}... 10µs
- N_{ovsa}... Oversampling factor according to

$$f_s = N_{ovsa} f_{B,max}$$

Fraction of consumed energy

$$\zeta(\eta) = \frac{E_{total}(\eta)}{E_{total}(1)} = \frac{\eta + \gamma}{1 + \gamma}$$

$$\gamma \approx \frac{I_{digital} N_{ovsa} N_{bit}}{I_{analog} f_s T_{burst}}$$

Energy Consumption analysis

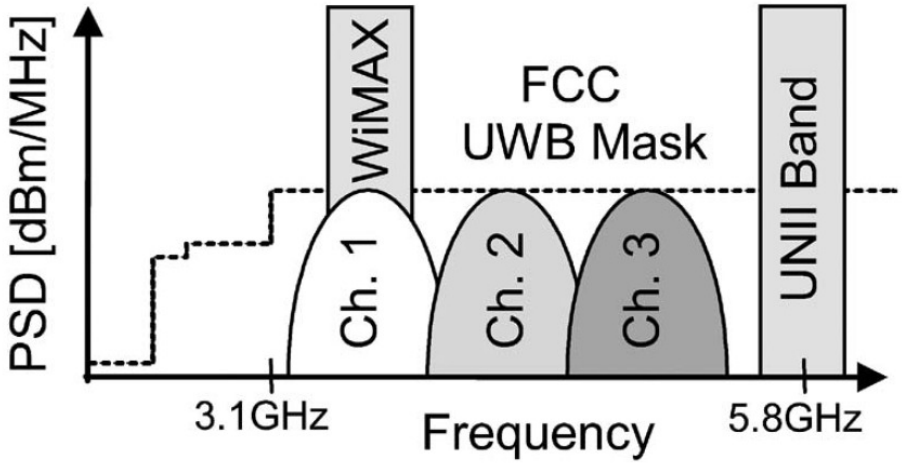
- Analog Parts
  - LNA, VGA, Squaring device, ADC, clock generation
  - The analog power consumption scales with the duty-cycle

$$I_{\text{analog}} = I_{\text{LNA}} + 2 \cdot I_{\text{Amp}} + I_{\text{Mix}} + I_{\text{ADC}} + I_{\text{s}} \approx 24.5 \text{ mA}$$

- Digital Parts
  - Complexity: 124 additions, 12 MAC's → 9.6 mA
  - SRAM: 10 mA
  - 19.6 mA at 200 MHz
- Overall energy consumption
  - Needed fraction of power $\zeta = 0.018$
  - **98 % of the power can be saved with a 1% duty-cycle**
  - 0.45 mA overall current consumption
  - 0.81 mW for 1.8 V supply → **1.6 nJ/Bit**

2nd design: UWB transceiver in 90nm

- From MIT
- Expensive process technology
- Three frequency bands for interference avoidance and multi-user diversity
- Up to 16.7 Mbps
- Pulse BW: 500 MHz
- 0.65 V supply voltage
- 2.5 nJ/Bit



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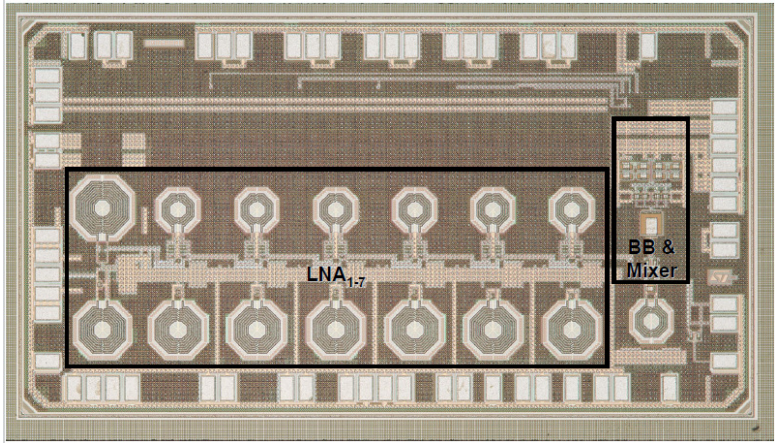

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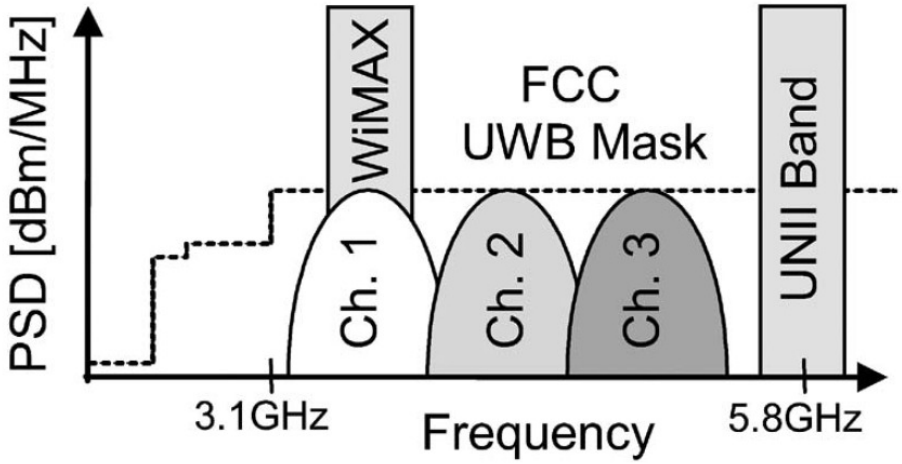

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Comparison

Main Publisher	nJ/Bit	MBit/s	max. MBit/s	Chip size	Technology
Stoica ‘05 (Univ. of Oulu)	2,7	0,005	5	2.65 mm²	0.18µm BiCMOS
Trösch ’07 (ETH)	1,6	0.5	50	*Not build yet*	0.18µm BiCMOS
Chandrakasan ’07 (MIT)	2,5	0.1	16.7	2.2 mm²	90nm CMOS

Comparsion to other Technologies

- ZigBee: 20mA for 100 kbps (360 nJ/b at 1.8V)
- Bluetooth: 30mA for 300 kbps (180 nJ/b at 1.8V)
- WLAN: 100mA for 10 Mbps (18 nJ/b at 1.8V)
- WUSB (Highspeed UWB): 200mA for 100 Mbps (3.6 nJ/b at 1.8V)

Conclusion

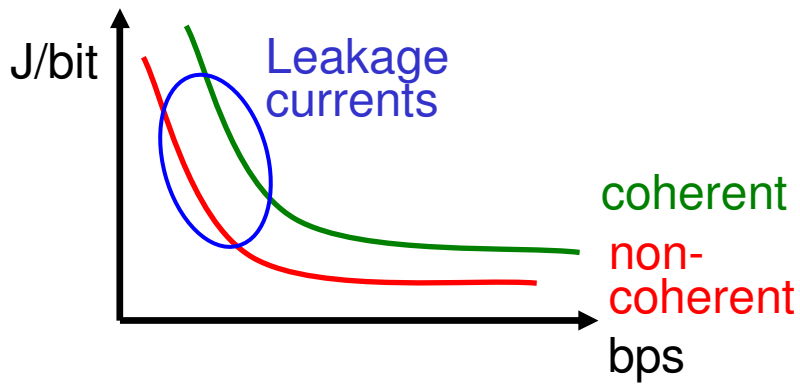
What mainly influences the energy consumption?

- Duty cycle reduction
- Hardware complexity / Process Technology
- Supply voltage
- Precision of pulse detection

Keep in mind

- Tradeoff btw. duty cycle reduction and link margin
- Independency of data-rate
- Amount of integrators determine the time accuracy

„Thank you for your attention!“



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[Stoi] L. Stoica, A. Rabbachin, H. Repo, T. Tiuraniemi, and I. Oppermann, “An ultrawideband system architecture for tag based wireless sensor networks,” IEEE Trans. Veh. Technol., vol. 54, no. 5, pp. 1632–1645, Sep. 2005

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