



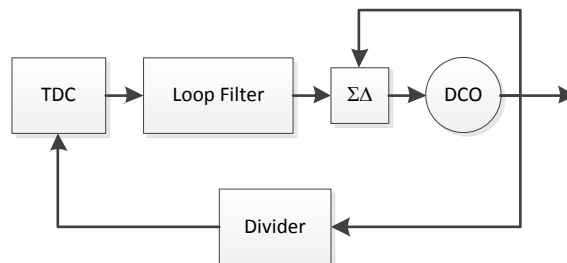
Proposal Master Thesis at INTEL

Thema / Topic:

Ereignisgesteuerte Simulation einer digitalen PLL in Matlab

Beschreibung / Description:

Für Entwurf und Analyse von digitalen Phasenregelkreisen (PLL) werden häufig Matlab code basierte Simulationen eingesetzt. Diese Beschreibungsart wird jedoch sehr komplex, wenn gegeneinander laufende (asynchrone) Taktdomänen in einer hochperformanten gemeinsamen Simulation betrachtet werden sollen. Abhilfe könnte eine ereignisgesteuerte Simulation bringen, welche einerseits die exakte Verarbeitung von Taktflanken gewährleistet, und andererseits eine einfache Modellierung der asynchronen Zeitereignisse erlaubt.



Ziel der Arbeit ist, ähnlich zu bereits existierenden Simulatoren eine ereignisgesteuerte Simulations-Maschine in Matlab zu implementieren. Diese soll auf eine einfache digitale PLL angewendet werden, und die damit erreichbare Performance gemessen werden.

Kontakt / Contact:

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Qualifikation / Qualification:

- Gute Kenntnisse in Matlab, Nachrichtentechnik



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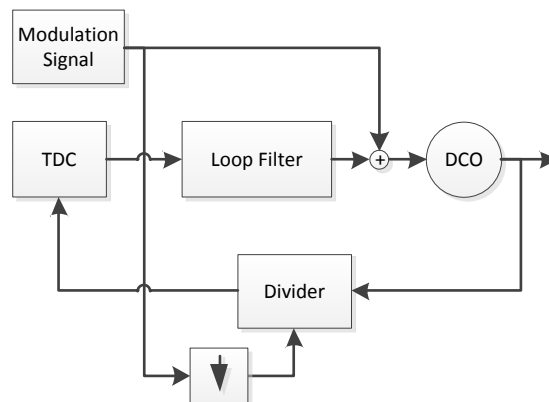
Thema / Topic:

Effects of Multi-rate Modulation in a Digital PLL Two-point Modulator

Beschreibung / Description:

RF Phase modulators in state of the art communication devices use a Digital PLL with two-point modulation scheme to provide high modulation bandwidth. Both paths have to match accurately in order to guarantee distortion-free modulation. However, due to the different sample rates of the two insertion points, exact matching is not possible.

Actual implementations show that the reached performance is sufficient, but future communication standards demand even higher bandwidths which make matching accuracy increasingly important.



The goal of this work is:

- Generate a discrete time model of the combined modulation paths
- Show the modulation transfer function and prove with time domain simulation
- Check influences on actual modulation standards
- Estimate bandwidth limitations of an existing phase modulator
- (optional) Propose modifications to overcome limitations

Kontakt / Contact:

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Qualifikation / Qualification:

- Matlab, Communications Engineering, Control Engineering, Digital Signal Processing

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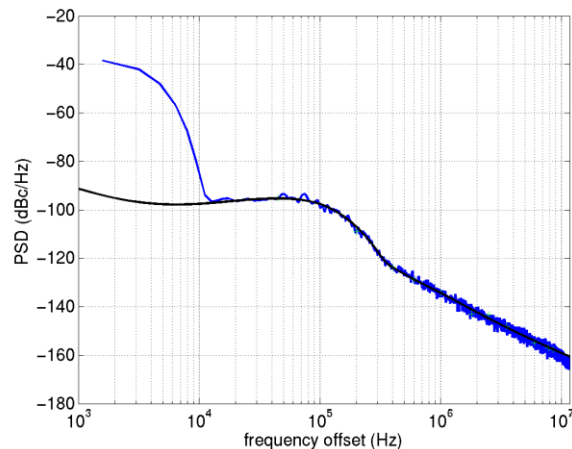
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Thema / Topic:

Optimal Digital Loop Filter in the Presence of Excess Loop Delay

Beschreibung / Description:

The noise transfer function of RF Digital Phase locked loops (PLL) used in state of the art communication devices is one part which defines the purity of the generated RF output signal. Digital signal processing in digital PLLs adds latency to the loop which reduces the achievable phase margin and leads to phase peaking of the closed loop transfer function. Actually used loop filter types do not take this delay into account. So the application of modern control theory considering the latency could help to find an optimized loop filter which enables higher performance needed for future high data rate communication standards.



The goal of this work is:

- Derive an alternative loop filter topology which takes into account latency of the loop
- Compare the noise transfer function of the new filter with the existing solution
- (optional) Give a proposal for loop filter implementation

Kontakt / Contact:

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Qualifikation / Qualification:

- Control Engineering, Digital Signal Processing, Matlab

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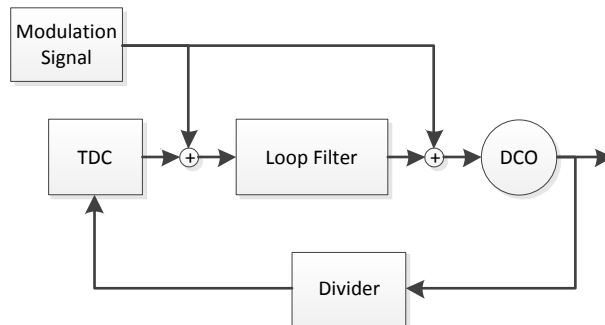
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Thema / Topic:

Effect of TDC nonlinearity on Modulation Quality in a Two-point Modulation Digital PLL

Beschreibung / Description:

Two-point modulation in a digital phase locked loop (PLL) enables high modulation bandwidths required for polar modulation in high data rate communication standards. If the low-pass path of the modulator is implemented after the time-to-digital converter (TDC), the nonlinearity of the TDC adds distortion to the modulation. A certain distortion is acceptable, but the limit of how much nonlinearity can be allowed and the specific effects on EVM and spectrum are not known yet.



The goal of this work is:

- Simulate a digital PLL two-point modulator in Matlab with a nonlinear TDC
- Show effect of nonlinearity on Error Vector Magnitude (EVM) and Spectrum

Kontakt / Contact:

Dr. Thomas Mayer - E-Mail: thomas.mayer@intel.com

Qualifikation / Qualification:

- Communications Engineering, Control Engineering, Digital Signal Processing, good knowledge of Matlab



Proposal Master Thesis at INTEL

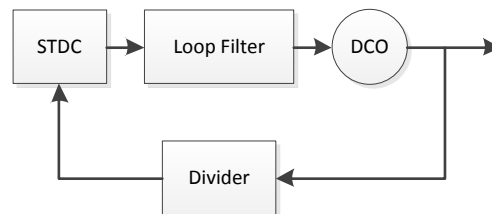
Thema / Topic:

Simulation of a Stochastic TDC for Divider Based PLLs

Beschreibung / Description:

Continuous increase of data rates in modern mobile communication standards set demands of improved purity of the generated RF signals. A limiting factor for the achievable purity is the in-band noise of the Phase Locked Loop (PLL). As the use of digital PLLs is preferred in advanced CMOS technologies, the Time-to-Digital Converter (TDC) quantization noise is the main contributor to the in-band noise. An approach to realize very fine quantization is the Stochastic TDC, which makes use of statistical properties of parallel switching elements in order to detect and quantize a time delay. However, stochastic TDCs can only resolve very short time delays, so a circuit is required to extend the limited detection range.

Proposals for such circuits exist, but they have to be analyzed in the application of divider based PLLs.



The goal of this work is:

- Generate a Matlab time domain model of a stochastic TDC which can be used in a divider based PLL
- Simulate the TDC within an existing time domain PLL model
- Identify limitations considering circuit imperfections

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Qualifikation / Qualification:

- Good knowledge of Matlab, Digital Signal Processing, Mixed Signal Circuit Design