Master Project

A Memristor Based all-analog UWB Receiver

conducted at the
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Graz University of Technology, Austria

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Statutory Declaration

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

date	(signature)

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1 Introduction and Motivation

Ultra-wide-band communication has been a recent topic in signal processing for the last years. The possibility to transmit data with a very high rate over a short distance is needed in many fields of applications like indoor positioning, imaging or wireless communication. It has a lot of advantages to established wireless communication systems as bluetooth and 802.11. However using large bandwidths of 500MHz and more in the 3-10GHz band by transmitting pulses of a very short duration of around one nanosecond makes decoding a real challenge. As digital signal processing systems are hardly capable of such high sampling rates and processing speeds, and all-analog approach has been made to solve this problem in [1]. This approach uses memristors to decode the received signal. The existence of the memristor has been predicted in the 1970s by L. Chua [2]. However it took more than 30 years until the first working memristor has been presented by HP Labs in 2008 [3]. The proposed solution shows the basic idea of such an analogue receiver, however does not go farther into detail when concerning realization and robustness. So the task for this project was to investigate the practicability of such a circuit. As there is no real memristor available for experimenting yet, the work is baled on MATLAB simulations.

2 Fundamentals and Background of this Work

2.1 Memristor Basics

2.1.1 History

To understand the function of the proposed receiver, some basic knowledge about memristors and their way of operation is needed. There are many papers dealing with the details of this topic so I try to focus on the issues which are necessary in this context. In the early 70s Leonard Chua [2] discovered that there must be a fourth passive circuit element and described its properties. However it took almost forty years until in 2009 the researchers of HP Labs were able to build a first prototype of this circuit element [3]. A nanometer thin layer of doped titanium dioxyd is surrounded by two plate electrodes. One part of the titanium-dioxyd layer is doped with oxygen holes and the other part is undoped [Fig. 2.1]. As soon as an electric field gets applied to the titan layer, the dopants start to drift, the space-charge region moves and with it the conductance of the layer changes dependent of the field's direction. So the conductance of the device depends on the former happenings, which is the basic property of memory. Because of this and the fact that the part looks like a resistor in static observations, it got the name memristor for memory-resistor.

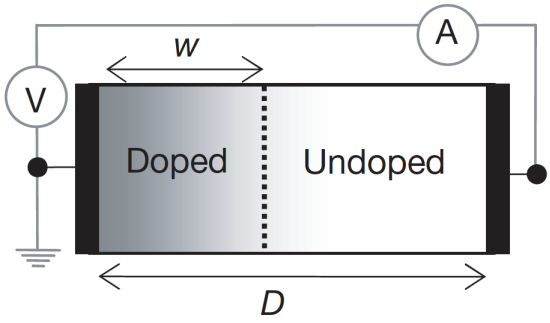


Figure 2.1: Receiver Circuit

2.1.2 Modeling

The simplest mathematical description for the behavior of the memristor is the voltage current relation:

$$v = M(w) * i \tag{2.1}$$

where

$$M(w) = R_{on}(\frac{w}{D}) + R_{off}(1 - \frac{w}{D}) \tag{2.2}$$

While R_{off} is the resistance of the device when the 'active' area is totally undoped, R_{on} is the resistance when the size of the doped region w is equal to the maximal size of this region D.

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{on}}{D} i(t) \tag{2.3}$$

From the first equation one can see that the static behavior of this memristor is comparable to a resistor but looking at the other equations, one can see that the dynamic behavior is quite different. As w depends on the current over the device, the memristance changes according to the flowing current. This model is called the *model with linear dopant drift* and is sufficient for some basic considerations as it reproduces the characteristic time hysteresis behavior. But for closer considerations this model is not sufficient. One major effect that is not modeled is the nonlinear dopant drift. In the linear model also small voltages over the device lead to quite large electric fields, which does not fit to the rules of electrodynamics. Another thing is the fact that in reality, no matter how much current flows over the device, the size of the doped region w will never get zero, because that would mean, that all oxygen vacancies would have vanished. The most used way to deal with those deficiencies, is to modify the formula to calculate $\frac{dw}{dt}$ by adding a nonlinear window function $f(x)$ where $x = \frac{w}{D}$. Two models where chosen to show the differences to the linear version:

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{on}}{D} i(t) f(\frac{w}{D}) \tag{2.4}$$

First the model of Biolek et al. [4] who proposed to choose the nonlinear window function by:

$$f(x) = 1 - (x - sgn(i))^{2p} \tag{2.5}$$

And second the model of Prodromakis [5] et al., where the window was defined as:

$$f(x) = j(1 - [(x - 0,5)^2 + 0,75)^p \tag{2.6}$$

Prodromakis' model has a high flexibility because of two freely adjustable scale factors, however the so called 'terminal state problem' occurs. When the width of the doped region reaches its minimum or maximum, the window function will get zero and the model gets stuck in this state forever. Biolek's model does not have this problem but suffers from discontinuities when the current changes direction. The suitability of both models for this particular case will be discussed later.

2.2 The analog UWB receiver

Using the properties of the memristor, a concept for an analog UWB receiver has been developed and published by Witrisal [1]. The main operation of this coherent, stored reference receiver is the correlation of a reference waveform with the received waveforms. The correlation operation

$$z(t) = \sum_{n=1}^{N} v_n(t_0) v_n(t) \tag{2.7}$$

of the reference signal $v_n(t_0)$ with the input signal $v_n(t)$ gets calculated and the output of this calculation can be directly used as decision variable. So multiplications and a summation have to be performed.

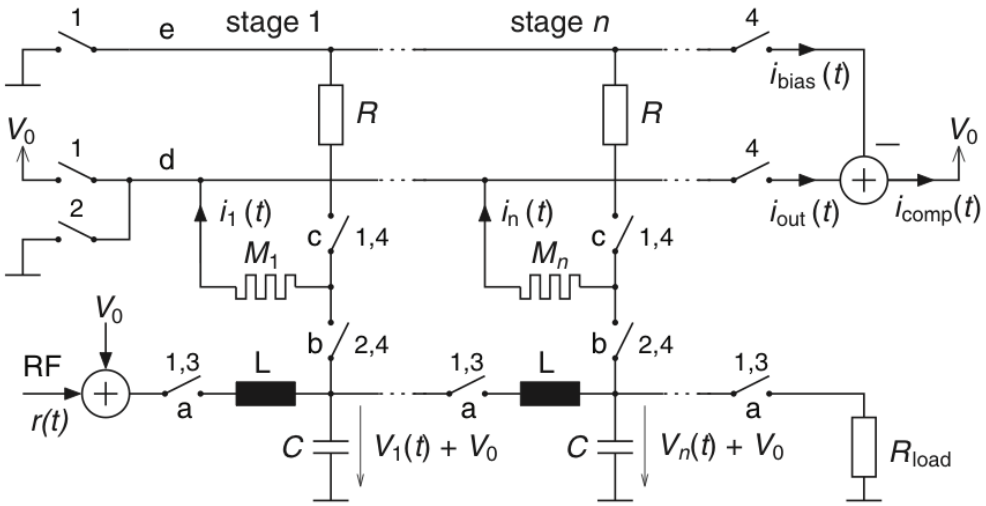


Figure 2.2: Receiver Circuit, see [1]

The receiver architecture as shown in the figure above consists of N equal stages, each processing the n-th part of the signal $v(t)$. The receiving process consists of four steps. In the first step the reference waveform gets stored in the N capacitors and at the same time all the memristors get set to a defined state by connecting one terminal to V_0 and the other one to ground for a sufficiently long time. In the second step the memristors get 'programmed' by the reference voltage stored in the capacitors, meaning that the memristance is set to a value proportional to V_{Cn}. Next the RF signal is passed through the transmission line which is step three. In the final step the switches marked with four get closed and the correlation result can be measured at the output in form of a current.

When the charge $V_0 + v_n(t_0)$ gets transferred over the memristors the n-th memristance can be written as

$$M_n = R_{off}(1 - \frac{\mu_v R_{on}}{D^2} C[V_0 + v_n(t_0)]) \tag{2.8}$$

By applying the voltage $v_n(t_0)$ to the memristor, the current equals

$$i_n(t) = v_n(t) \frac{1}{R_{off}} \frac{1}{1 - K[V_0 + v_n(t_0)]} \approx v_n(t) \frac{1}{R_{off}} (1 + K[V_0 + v_n(t_0)]) \quad where \quad K = \frac{\mu_v R_{on} C}{D^2} \tag{2.9}$$

and the sum of all currents is

$$i_{out}(t) = \frac{1}{R_{off}} \sum_{n=1}^{N} K v_n(t) v_n(t0) + (1 + K[V_0 v_n(t)]) \tag{2.10}$$

where one can clearly see that the required multiplication and summation has been performed.

3 Tasks and Simulation

As written above the task in this work is to analyze the proposed receiver concerning device tolerances and variations and to improve its robustness. For the simulations of the circuit, MATLAB has been chosen. First it is a very versatile and performant tool to build high level simulations and second it is quite easy to start with very general models and then expand them to more detailed and realistic models.

3.1 Input Signals and Channel Simulation

To test the function of the receiver, BPAM modulation has been chosen. The test signal consists of a reference pulse, which is used to program the memristors and after a break N data pulses get transmitted. The generated bit stream gets convolved with the estimated impulse response of a typical UWB transmission channel. Tab. 3.1 shows the timings used for the simulation.

name	value	description
T	10ns	symbol frequency
T_s	$50ps$	sampling frequency
T_g	$30ns$	guard interval after reference symbol
N	100	typical number of symbols

Table 3.1: Simulation Timings

3.2 Modeling the receiver

The basic version of the receiver is built to show the principle mechanism and uses some idealizations which will be investigated later. As mentioned above, one symbol has the duration of $10ns$. By using 200 stages, a time resolution of $50ps$ is achieved which is considered to be accurate enough to achieve a good performance of the receiver.

3.2.1 Settings

A proper selection of the components sizes has big influence on the performance of the receiver. The size of the capacitor has been chosen to be $1nF$ because this is the capacitance of a 50Ω segment that delays the signal by the desired $50ps$. Looking back to chapter 2 the output current is

$$i_{out}(t) = \frac{1}{R_{off}} \sum_{n=1}^{N} K v_n(t) v_n(t_0) + (1 + K[V_0 v_n(t)]) \tag{3.1}$$

so, if the resistance is chosen to equal to $R_{off}/(1 + V0)$, then the additive term vanishes and the output current is proportional to $K * v_n(t) * v_n(t_0)$ To put CR_{mem} to 10ns R_{off} has to be $10k\Omega$. To keep the linearization in equation (3.1) valid, $D = 3nm$ and $R_{on} = 100\Omega$ at a given $\mu_V = 3 * 10^{-8} \frac{nm}{Vs}$.

To keep the results of the different modifications of the circuit comparable, the basic values for the components chosen above are kept constant. Table 3.2 shows the basic settings which were used in all simulations unless otherwise specified:

name	value	description
R	9750Ω	compensation resitors
C	1 nF	storing capacitors
N	1000	number of symbols
V_0	0,2 V	bias voltage
Memristor		
R_{on}	100Ω	minimal memristance
R_{off}	$10k\Omega$	maximal resistance
μ_v	$100\frac{nm}{Vs}$	mobility of the carriers
D	$3nm$	maximal thickness of the doped area
model	2	used memristor model

Table 3.2: Used Simualation Settings

Using the model the following aspects of the receiver should be analyzed:

- different memristor models
- tolerances of the memristors, resistors and capacitances
- additive noise at the input
- multiple programming of the memristors
- transistor switches and charge injection errors

3.3 Measuring the performance

In order to determine the performance of the model, two measurement units where chosen. first the signal-to-noise ratio and second the level of the output current.

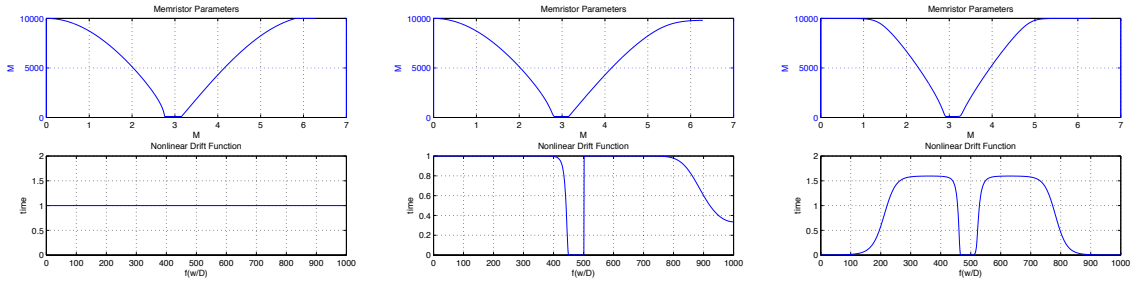
To decide whether a 1 or a -1 has been transmitted, the output current gets sampled at the time points where a maximum of the correlation should occur. The signal-to-noise ratio (SNR)

is calculated by the mean value of the output current at the sampling points multiplied by the value, they should represent $[+1, -1]$ over noise power which is the variance of the detected currents. The amplitude of the mean values is important to estimate the robustness of the receiver. The typical values with the choses settings is in the area of some μv, so a stronger output leads to higher robustness against outer influences.

4 Results and Discussion

4.1 Memristor Models

The first thing to investigate was the change in the performance of the receiver by using different memristor models. The nonlinear models have one respectively two parameters to be chosen. A careful selection of these parameters was necessary to obtain meaningful results. Literature gave some hints how to choose them and the fine adjustment has been done iteratively. Figure 4.1 shows memristor parameters (m and M) and the nonlinear function $f(w/D)$ of the three different models when stimulated with a sinusoidal signal:



(a) Linear Model (b) Biolek (c) Prodomakis

Figure 4.1: Different Memristor Models

Afterwards each of the models was plugged into the receiver model and the performance has been measured. As expected the linear model performs best because it reacts already on smallest voltages over the device while the other two models need a certain voltage to 'activate' the dopant drift. The performance of the nonlinear models can be adjusted by setting the parameters p and j which has high impact on the performance of the models. Which parameters were used to fit the physical memristor could not been found out, so the proposed parameters in the papers were used.

4.2 Additive Noise at the Input

This sections deals with the question, how much additive white noise at the input influences the performance of the receiver. There are two different cases which were taken into account.

Ideal reference pulse and noisy data pulses

First the reaction on the system to AWGN only added to the data pulses has been investigated while the reference pulse, which is used to program the receiver, is still kept ideal. To determine the energy of the noise in relation to the signal, the energy per bit has been measured and put in relation to the spectral noise energy of the signal. [6]

$$SNR_{dB} = 10log(\frac{\epsilon_b}{N_0}.\frac{f_B}{B}) \tag{4.1}$$

where f_b is the data rate and B is the bandwidth of the signal. The energy of the noise has been put between 0.1 times the bit energy to 10 times the bit energy. The results of the simulations can be seen in the figure below.

As one can see the noise suppression of the system is quite high in the beginning and the SNR of the receiver is still around 5dB with a SNR at the input of 0dB which looks promising but further investigation has been done in further work.

Noisy reference pulse and noisy data pulses

Now, in difference to the case before, the reference signal to program the receiver is not ideal any more but also corrupted by AWGN. As expected the result is worse but it still leads to useable results. At a input SNR of $10dB$ the output SNR is $3dB$ lower than with ideal reference signal. The decline by $3dB$ is the same for a input SNR of $0dB$

4.3 Component Tolerances

One main question of this work was to investigate robustness of the provided circuit. Probably the first question, that pops up if one is asked to realize the given circuit is what happens if the resistors and the capacitors are not ideal. Systematic and statistical tolerances where considered and simulated.

4.3.1 Statistical Tolerances

No matter how the resistors and capacitors get realized either as integrated circuit or with discrete parts, the performance will suffer from tolerances. In this first part, statistical tolerances are taken into account. Fig. 4.2 and Fig. 4.3 show the result of the simulations. As expected with increasing tolerances of the resistor, the performance in our case the SNR goes down. Surprisingly the measured SNR is still higher than 5dB even if the tolerances of the capacitances reach 10%.

The same is valid for tolerances of the Memristors and the Resistors but when the tolerances of the memristor rise, also some tolerance in the resistors seems to be required to compensate that, leading to a higher SNR as it can be seen in the figure below. Further the systems is more sensitive to rising tolerances of the Memristor, a variance of 6% leads already to a decrease of the SNR to approximately $5dB$.

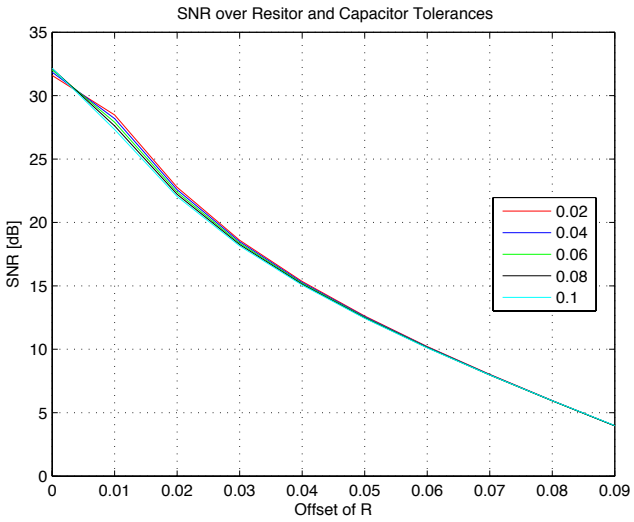


Figure 4.2: Statistical Offset of R and C

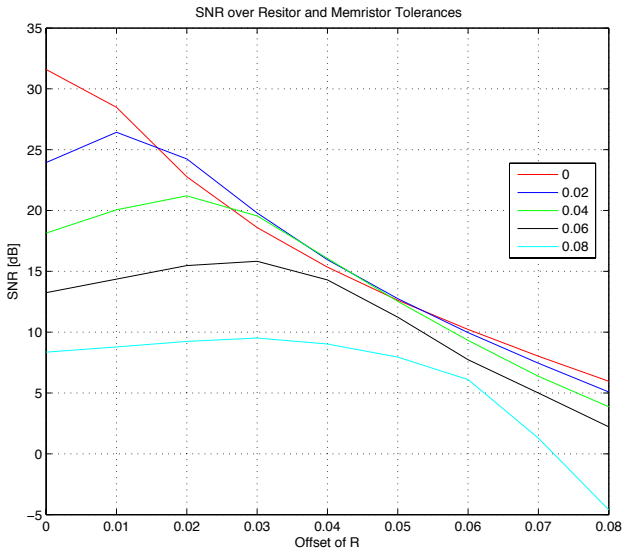
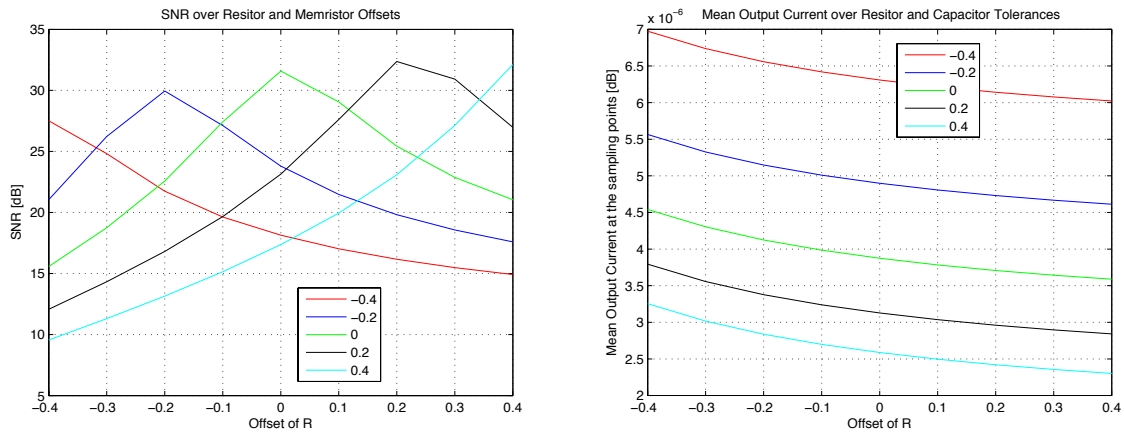


Figure 4.3: Statistical Offset of R and M

4.3.2 Systematic Tolerances

In difference to the statistical tolerances, also systematic offsets were investigated to maybe find better parameters for the devices. It was performed with the capacitors resistors and memristors. Interested results were achieved in varying R and M. The best performance is being achieved when R and M fit to each other as calculated in the chapter before, because the ideal fit resistance eliminates the distortion term best. However the smaller M and R are chosen the better is the output signal which is also obvious as the voltages stay the same and with smaller resistances it leads to larger output currents.

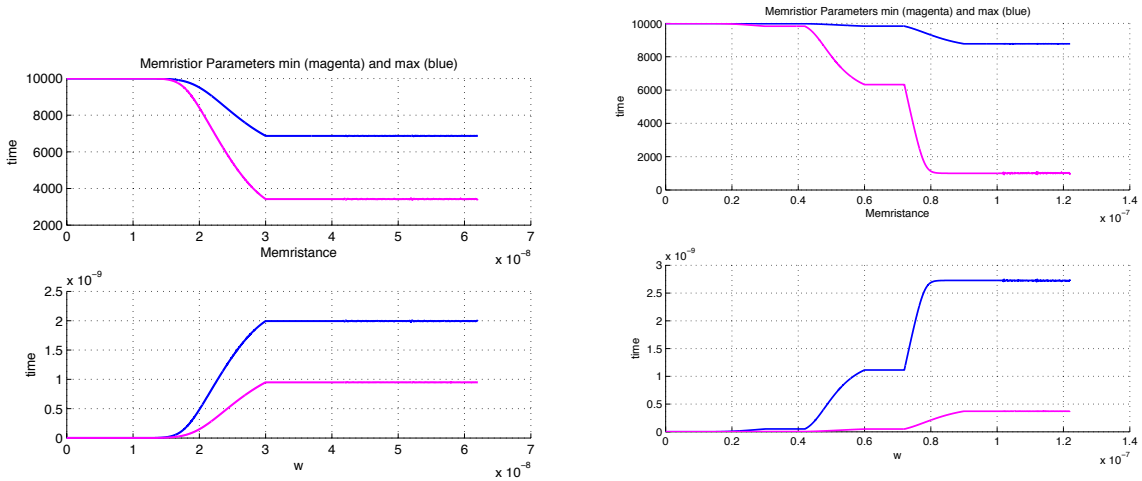


(a) SNR (b) Mean

Figure 4.4: Systematic Offset of R and M

4.4 Multi Charging of the Memristor

One approach to increase the robustness of the circuit is already mentioned in the original paper. When the phases two and three of the receiving process is repeated multiple times, which are the phases where the memristances get set by applying the reference waveform to the memristors. The disadvantage of this process is the much larger time needed to set the receiver which has to be set in relation to the higher output signal. Another big advantage is that nor any modification in the present hardware neither additional hardware is needed to increase the performance.



(a) One charge transfer (b) Three charge transfers

Figure 4.5: Memristance and w

The multi charging leads to a way bigger difference between the minimal and maximal memristance as it is shown in Fig. 4.5. which leads to a stronger output current. While the output current gets increased, the SNR dos not improve significantly [Tab. 4.1]. The number of maximal charges has to be chosen according to the chosen offset voltages. Too high offset voltages and too many charges lead to a saturation of single memristors and a rapid decrease in performance.

charge transfers	SNR	output current
1	38,27 dB	0,317 mA
2	37,16 dB	0,624 mA
2	33,6 dB	0,980 mA

Table 4.1: performance with different program cycles

4.5 Real Switches and Charge Injection Errors

In the simulations before the switches in the circuit were assumed to be ideal. Now those ideal switches are replaced by transistors respectively their models. To keep the simulation easy and as they are sufficient for this case only simple transistor equations were used [7]. The -3dB frequency should be 20 GHz so the with a capacitance of $1pF$ the drain-source resistance to the transistor should be smaller than $7,9\Omega$ which is equal to $\frac{V_{ds}}{I_{ds}}$ where

$$I_d = \frac{\mu_n * C_{ox}}{2}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{4.2}$$

name	value	description
$\mu_n C_{ox}$	$92\frac{\mu A}{V^2}$	carrier mobility * oxide capacitence
L_{min}	$0,18\mu m$	minimal transistor length
V_{gs}	1V	gate-source voltage
V_{th}	0,6V	threshold voltage

Table 4.2: Used Transistor Parameters

with the parameters from Tab. 4.2, the width of the transistor must be $20,83\mu m$

As the switches in the circuit are realized as transistors charge injection has to be taken in account at such small signal voltages. When a transistor gets turned off two mechanisms cause charge errors. The first is due to the channel charge which has to flow out of the channel into drain and source and causes a raise in voltage there. The second reason is the charge from the over lab capacitances between gate and source. As the second mechanism is way small than the first one, only the first one is taken into account.

$$\Delta V = -\frac{(V_{gs} - V_{th})C_{ox} * W * L}{2C} \tag{4.3}$$

So each transistor switch off, rises the voltage in the capacitors by $-2,2mV$. The charge injection together with the effect of the used transistor equations on the circuit the performance achieved decreases rapidly, from $24,84dB$ to $14,19dB$.

5 Discussion and Outlook

The basic question of the work which was to investigate the robustness and realizability of the proposed receiver could mainly be answered. The performance of the different memristor models strongly depend on the chosen parameters, where it was impossible to find the right ones to fit the physical memristor as good as possible. A universal model taking all of the key-effects in account, has not been found yet.
The robustness against input noise and device tolerances is in an acceptable range to keep the performance of the proposed circuit up. Multiple memristor programming has already been proposed in the original paper and really leads to better performance of the receiver. Long term stability or the need for reprogramming with the reference signal to react on a changing channel has not been taken into account. Also the, first ideal, delay line has only been changed to a bucket-brigade-device with basically modeled transistors. A CCD delay line, respectively its model, can lead to better performance. Concluding one can say that the investigations led to quite positive results and further work on this topic can be done.

As the time for such a project is quite short, not all the interesting questions could be answered. Further tasks could improve the memristor models or build up a prototype with real building parts and a memristor emulator, where the speed is due to the speed of available hardware has to be scaled down by several magnitude decades.

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